

1 1

1 2

サンプル	研磨レート (A/min)	均一性 (%)	平坦化特性 0-加段差(A)	底部削れ量(A)	耐久性
実施例 1	900	3	60	900	1000 枚
実施例 2	850	6	40	750	2500 枚
実施例 3	870	4.5	50	800	1100 枚
実施例 4	920	4.5	50	800	950 枚
実施例 5	900	3	60	900	1000 枚
実施例 6	850	3	60	900	1000 枚
比較例 1	840	11	70	1050	4000 枚
比較例 2	930	3	30	700	300 枚
比較例 3	870	12	40	750	1100 枚
比較例 4	700	3	60	900	1100 枚

【0025】

10* 【図1】本発明の研磨パッドの断面図である

【発明の効果】本発明の研磨パッドを各種の研磨に用いることにより、高い研磨速度を維持しながら、平坦性、均一性共に優れた被研磨物を得ることが出来る。

【符号の説明】

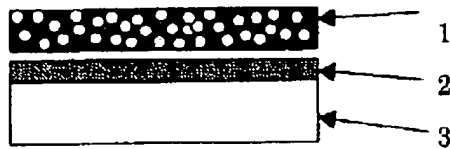
1：表面研磨層（発泡ポリウレタン）

2：高弾性層（PET、発泡PET層）

【図面の簡単な説明】

* 3：柔らかい層

【図1】



フロントページの続き

(72)発明者 小野 浩一

滋賀県大津市堅田二丁目1番1号 東洋紡
績株式会社総合研究所内

Fターム(参考) 3C058 AA09 CB01 CB02 CB10 DA12
DA17

PAT-NO: JP02002075933A
DOCUMENT-IDENTIFIER: JP 2002075933 A
TITLE: POLISHING PAD
PUBN-DATE: March 15, 2002

INVENTOR-INFORMATION:

NAME	COUNTRY
SHIMOMURA, TETSUO	N/A
NAKAMORI, MASAHIKO	N/A
KOMAI, SHIGERU	N/A
ONO, KOICHI	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOYOBO CO LTD	N/A

APPL-NO: JP2000252832

APPL-DATE: August 23, 2000

INT-CL (IPC): H01L021/304, B24B037/00

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a polishing pad for polishing semiconductor wafer capable of meeting conflict requirement of uniformity of polishing degree all over the wafer and planarization characteristic of concavity and convexity of micro region in the polishing process for planarizing concavity and convexity of micro pattern formed on the semiconductor wafer.

SOLUTION: The polishing pad for polishing semiconductor wafer with patterns formed on its surface and having micro concavity and convexity comprises a polishing layer 1 of the pad with its most surface layer formed by porous elastic resin layer, a resin layer 2 (second layer) adjoining the

porous
elastic resin layer and having greater degree of elasticity than the
same, and
a layer 3 (third layer) laminated on the opposite side of the porous
elastic
resin layer from the second layer and softer enough than the second
layer.

COPYRIGHT: (C) 2002, JPO

DERWENT-ACC-NO: 2002-447384

DERWENT-WEEK: 200248

COPYRIGHT 2005 DERWENT INFORMATION LTD

TITLE: Polishing pad for semiconductor wafer, has
soft layer
with elasticity lower than PET layer, which is
laminated
on reverse side of PET layer

PATENT-ASSIGNEE: TOYOBO KK[TOYM]

PRIORITY-DATA: 2000JP-0252832 (August 23, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
PAGES MAIN-IPC		
<u>JP 2002075933</u> A	March 15, 2002	N/A
007 H01L 021/304		

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO
APPL-DATE		
JP2002075933A	N/A	2000JP-0252832
August 23, 2000		

INT-CL (IPC): B24B037/00, H01L021/304

ABSTRACTED-PUB-NO: JP2002075933A

BASIC-ABSTRACT:

NOVELTY - A foam PET layer (2) with elasticity higher than a polish layer (1) having a foam polyurethane, is formed on the polish layer. A soft layer (3) with elasticity lower than the PET layer, is laminated on the reverse side of the PET layer.

USE - Used for polishing semiconductor wafer.

ADVANTAGE - Maintains high polishing velocity, by using the polishing pad for various polishing. Uniform polishing is enhanced.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the polishing pad.

Polish layer 1

Foam PET layer 2

Soft layer 3

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: POLISH PAD SEMICONDUCTOR WAFER SOFT LAYER ELASTIC LOWER PET LAYER

LAMINATE REVERSE SIDE PET LAYER

DERWENT-CLASS: A85 L03 P61 U11

CPI-CODES: A99-A; L04-B04A;

EPI-CODES: U11-C06A1A;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2002-127741

Non-CPI Secondary Accession Numbers: N2002-352550